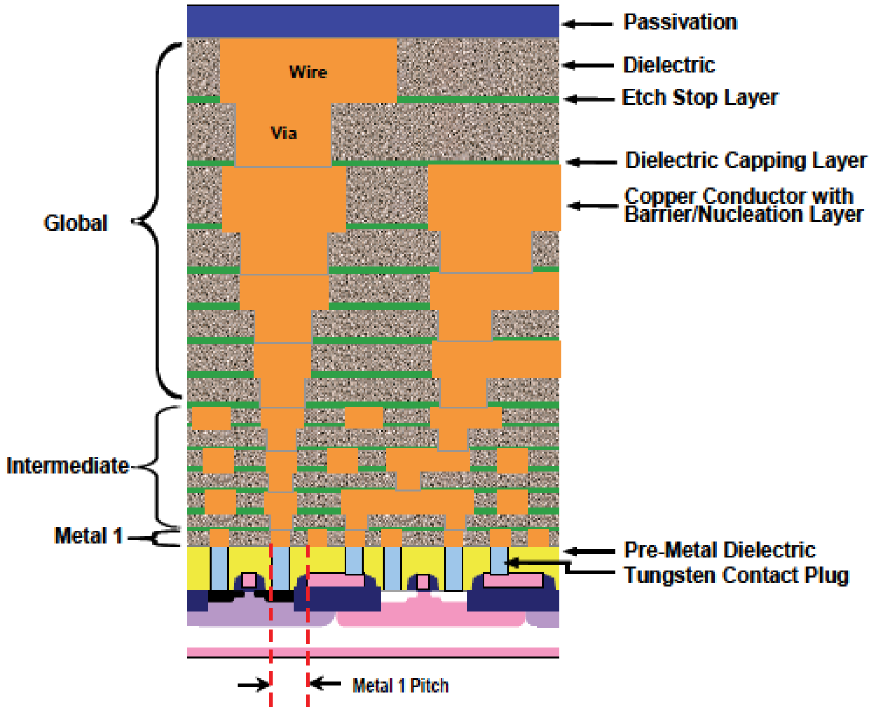
Outline

- A New Manufacturing Process for Fabricating 3-D Interconnects for MEMS and ICs
  - Why Stacking 3-D Interconnects
  - Challenges in Conventional 3-D Interconnect Manufacturing
  - A New Way of Manufacturing Micro/Nano Scale Interconnects
- Flex Introduction
  - Industries and Products
  - Innovation at Flex
  - Boston Innovation Center

Why 3-D Stacking of Interconnects

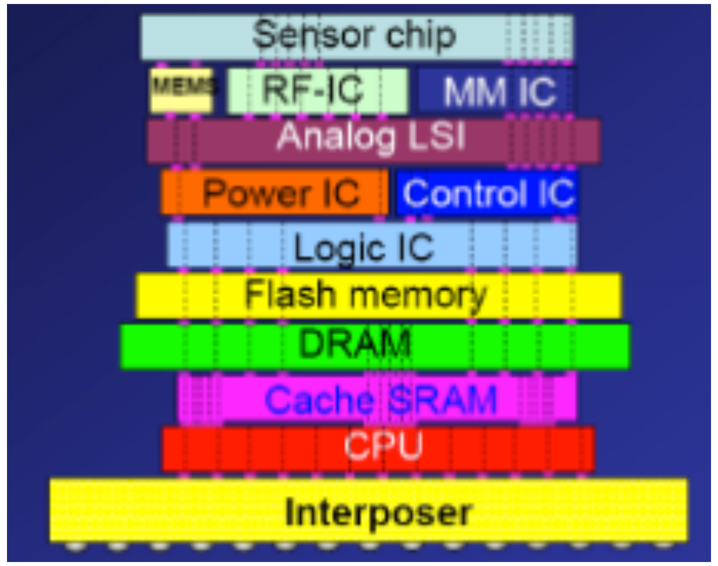
➢ Miniaturization



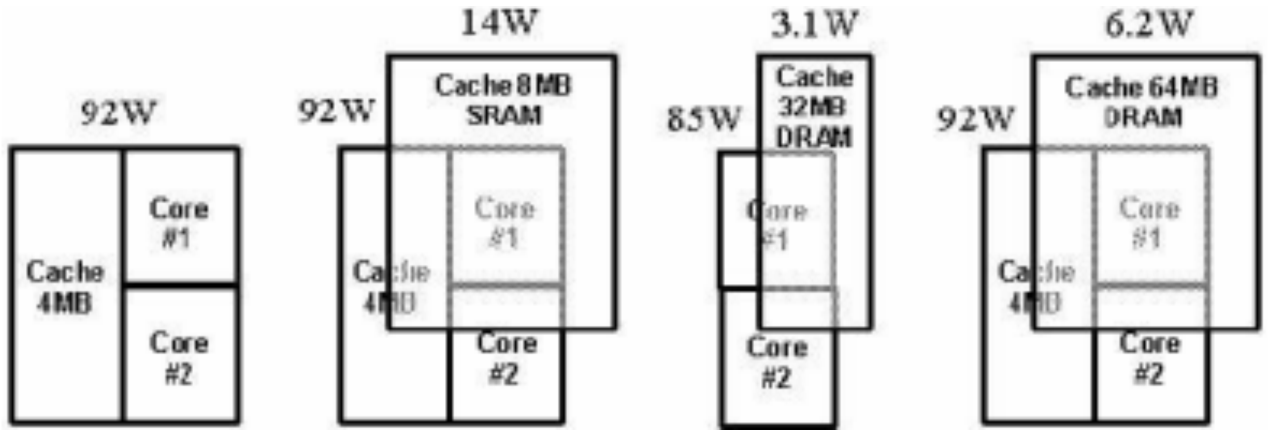
International Technology Roadmap for Semiconductors, 2007 Edition, Interconnect, pp. 5.

➢ Functionality

Heterogeneous Integration



➢ Enhanced Performance

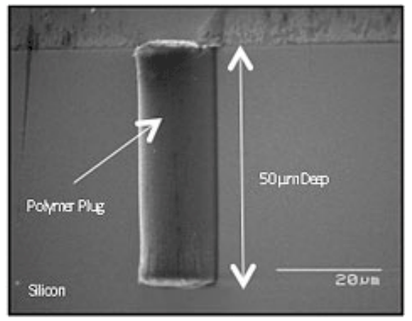


Significant power consumption

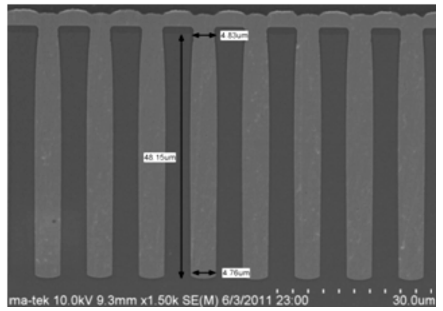
Source: Intel

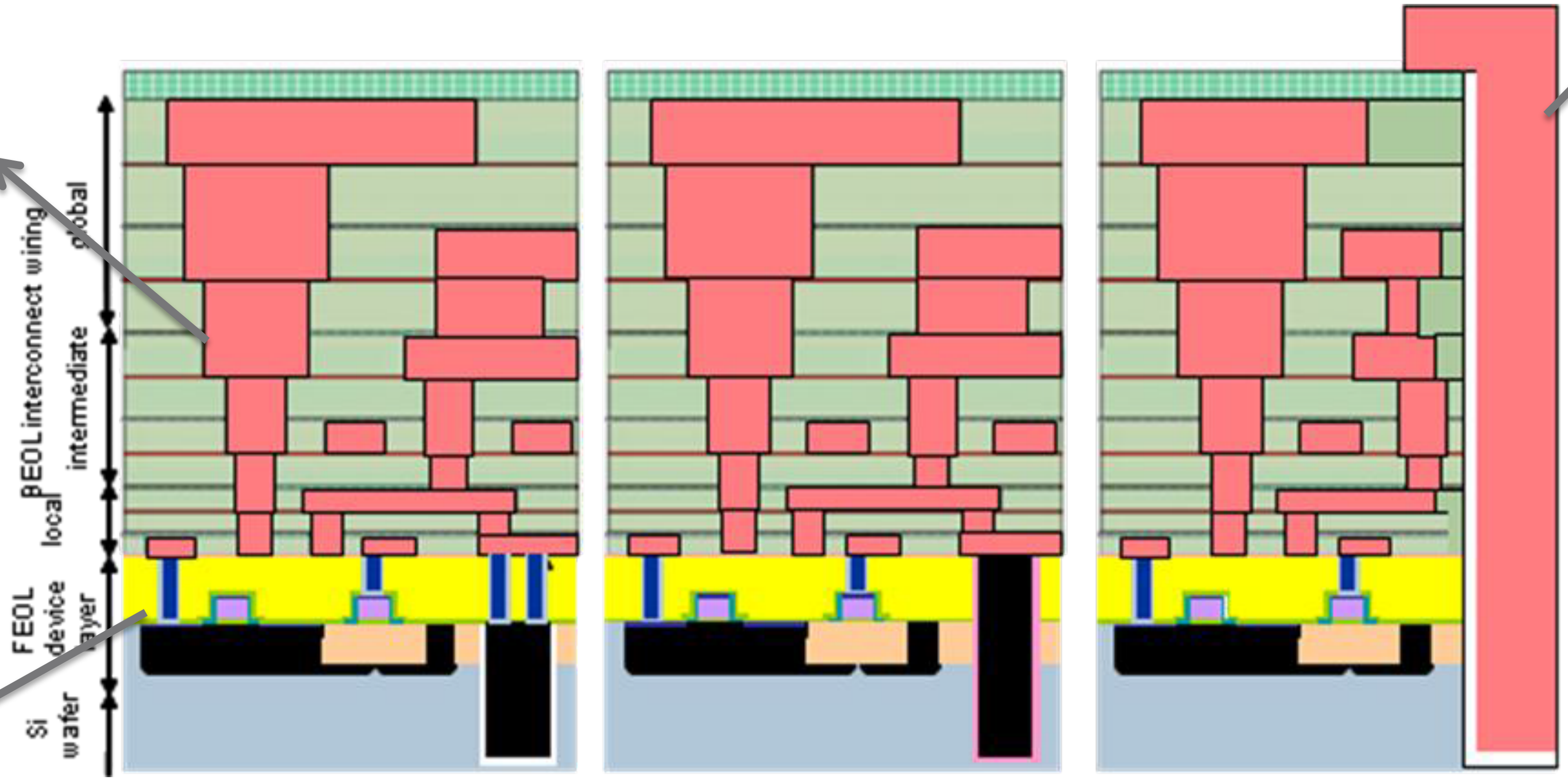
3-D Interconnects for IC and MEMS

Wafer packaging level interconnects (8-10μm)

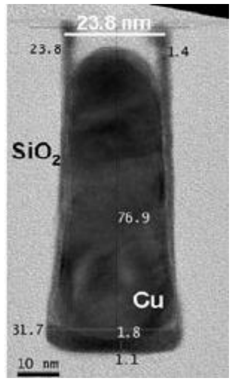


Global interconnects (1-2μm)





Local interconnects (<22nm)

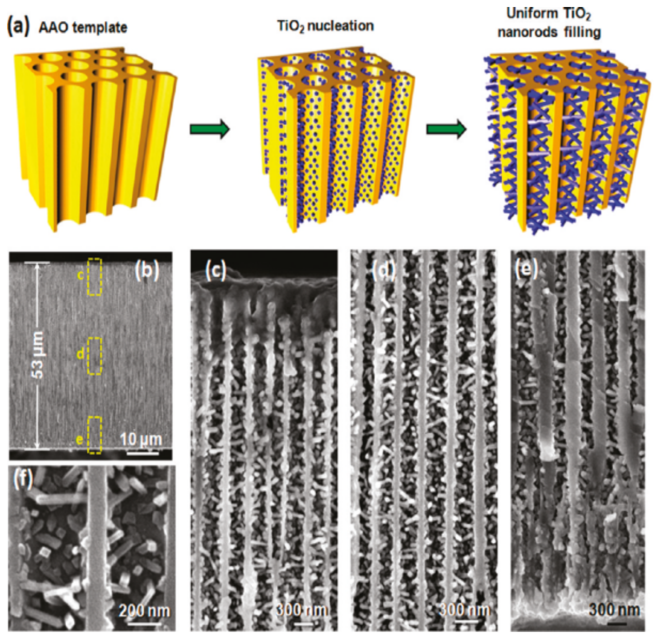


Schematic Crosssections of TSV First and Middle/Last

International Technology Roadmap for Semiconductors, 2007 Edition, Interconnect, pp. 5.

Conventional 3-D Interconnect Fabrication Methods

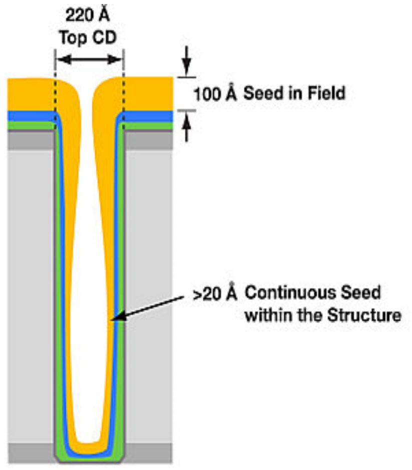
Chemical vapor deposition

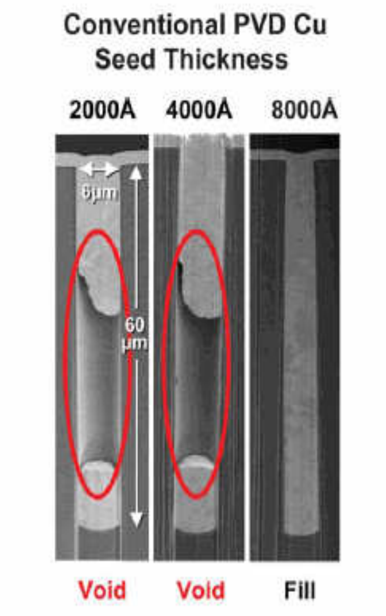


High temperature, high vacuum, difficult of control dimensions at nanoscale

Jian Shi et al.,Nano Lett. 2011, 11, 624–631

Physical vapor deposition

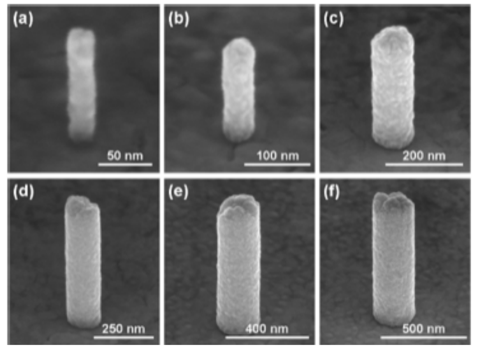




Novellus systems Inc.

High vacuum, non-uniform deposition at nanoscale

Electrochemical deposition



Michael J. Burek et al., Nano Lett. , 10, 2010

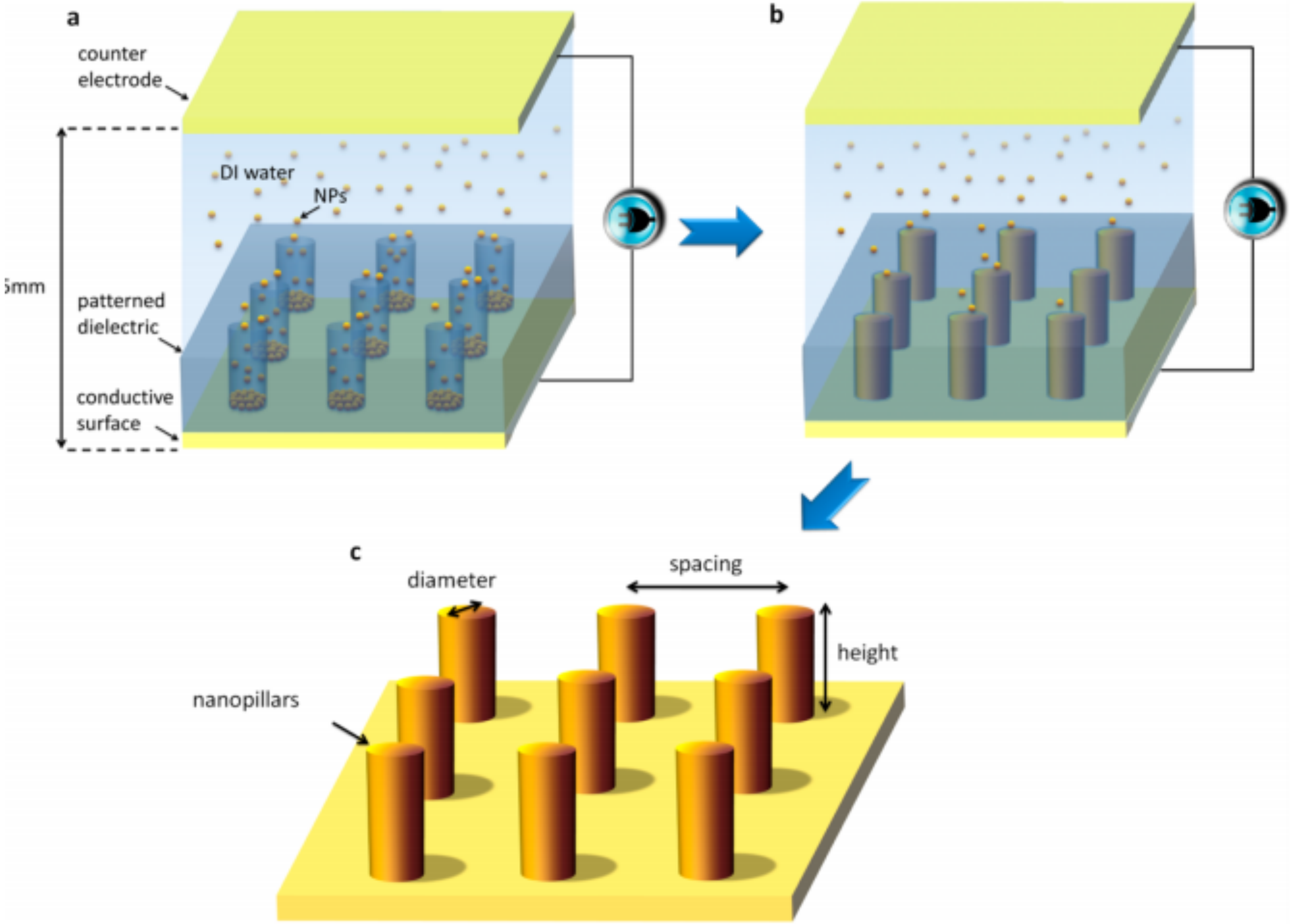
Complex chemistry, seed layer, non-uniform at nanoscale and costly at larger scales

What is the Need for Next Generation 3-D Interconnects?

There is a need for an alternative interconnect fabrication processes to address the challenges of fabricating 3-D interconnect for MEMS and IC.

- **Scalable to nano and micro dimensions**
- **Fast**
- **Applicable to wide range of materials**
- **Cost-effective**

Developed Method of Fabricating 3-D Interconnects



- Fast
- Scalable
- Room-temperature and pressure
- Chemical- free
- Cost-effective
- Environmentally friendly
- No need a seed layer
- Material independent
- Hybrid nanostructures

Forces Acting on the Particles under the applied AC Electric Field

Dielectrophoretic Froce:

$$F_{DEP} = 2\pi\varepsilon_1 \mathrm{Re}|\underline{K}(\omega)|r^3 \nabla E^2$$

$$\mathrm{Re}\,|\,K\,| = \frac{\varepsilon_2 - \varepsilon_1}{\varepsilon_2 + 2\varepsilon_1} + \frac{3(\varepsilon_1\sigma_2 - \varepsilon_2\sigma_1)}{\tau_{MW}(\sigma_2 + 2\sigma_1)^2(1 + \omega^2\tau_{MW}{}^2)}$$

$$\tau_{MW} = \frac{\varepsilon_2 + 2\varepsilon_1}{\sigma_2 + 2\sigma_1}$$

r is the radius of the particle

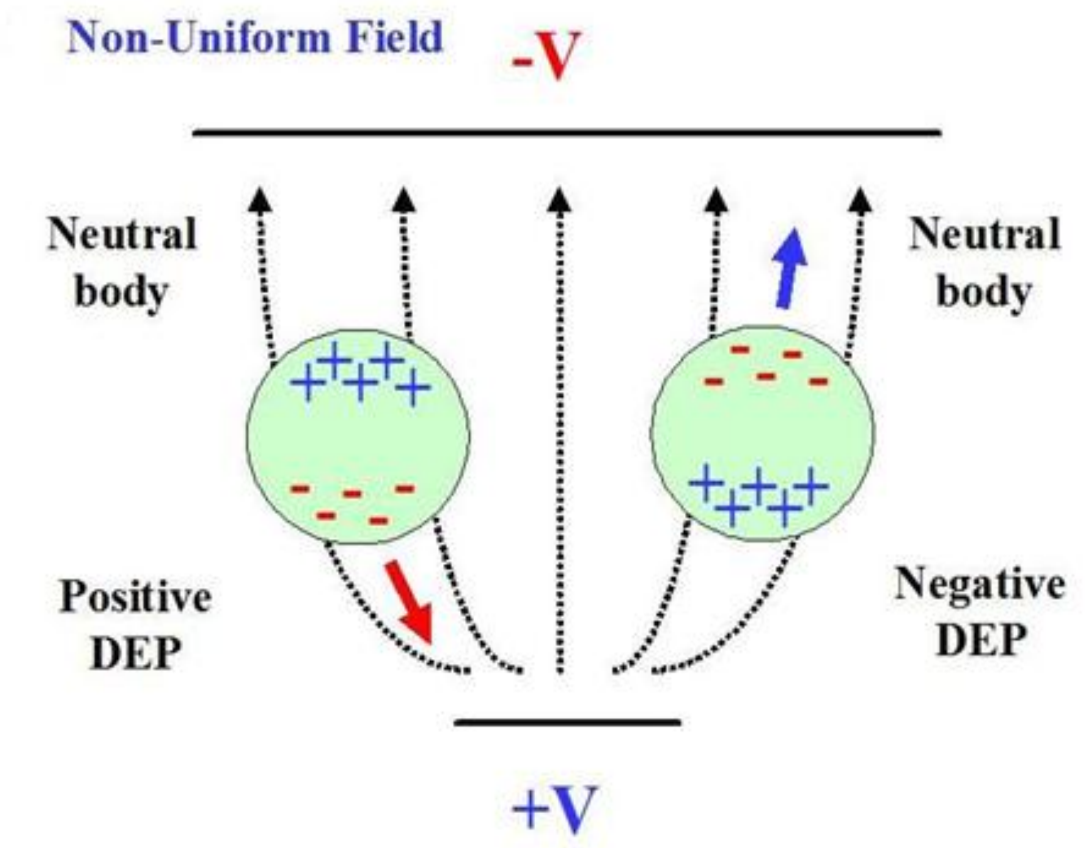
ε_1 dielectric permittivity of particle

ε_2 dielectric permittivity of medium

Re|*K*ω| is Clausius–Mossotti

Maxwell-Wagner charge relaxation time

$\varepsilon_1 > \varepsilon_2$ ➡ positive dielectrophoresis

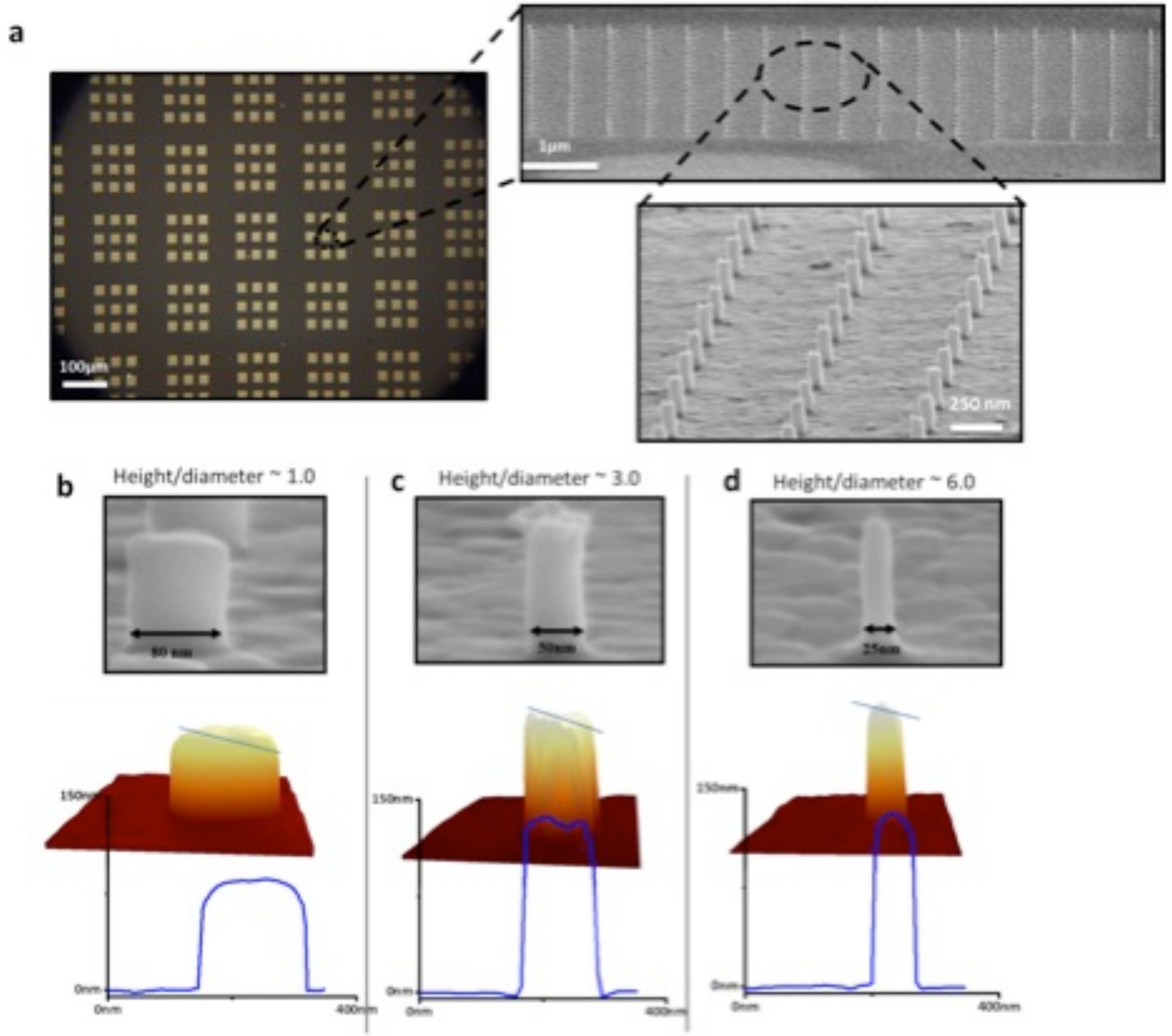


Dielectrophoresis and Optoelectronic Tweezers for Nanomanipulation, Stanford University, Jong Min Sung, December 10, 2007.

Governing Parameters

- voltage
- frequency
- particle size
- particle type
- particle concentration
- pattern dimensions
- assembly time
- solution pH and ionic strength

Fabrication of Interconnects with Controlled dimensions

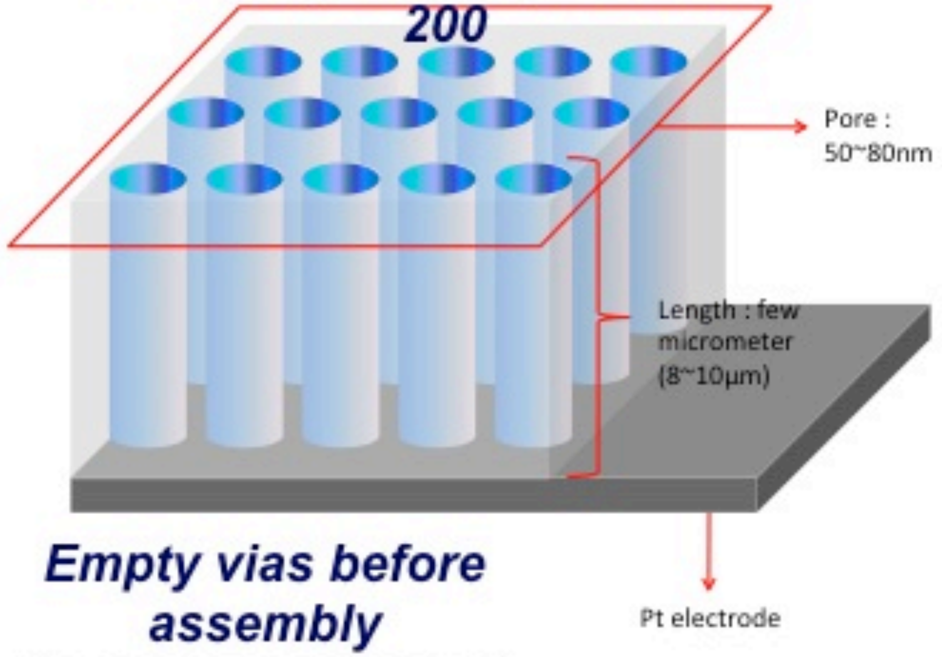


Cihan Yilmaz et al., **ACS Nano**, 2014, 8 (5), pp 4547–4558

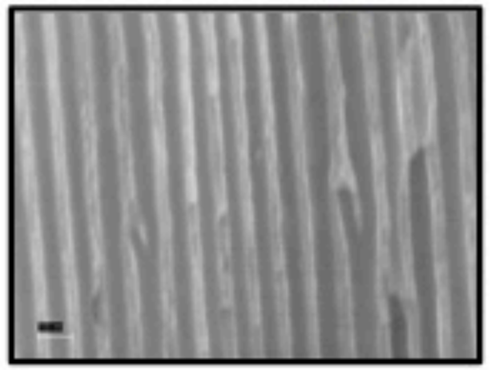
- ➢ **Fabrication over a large area. Uniformity is 90.3% over millimeters area.**
- ➢ **Controlled, repeatable and reliable fabrication.**

Fabrication of Interconnects in Very High Aspect Ratio Vias

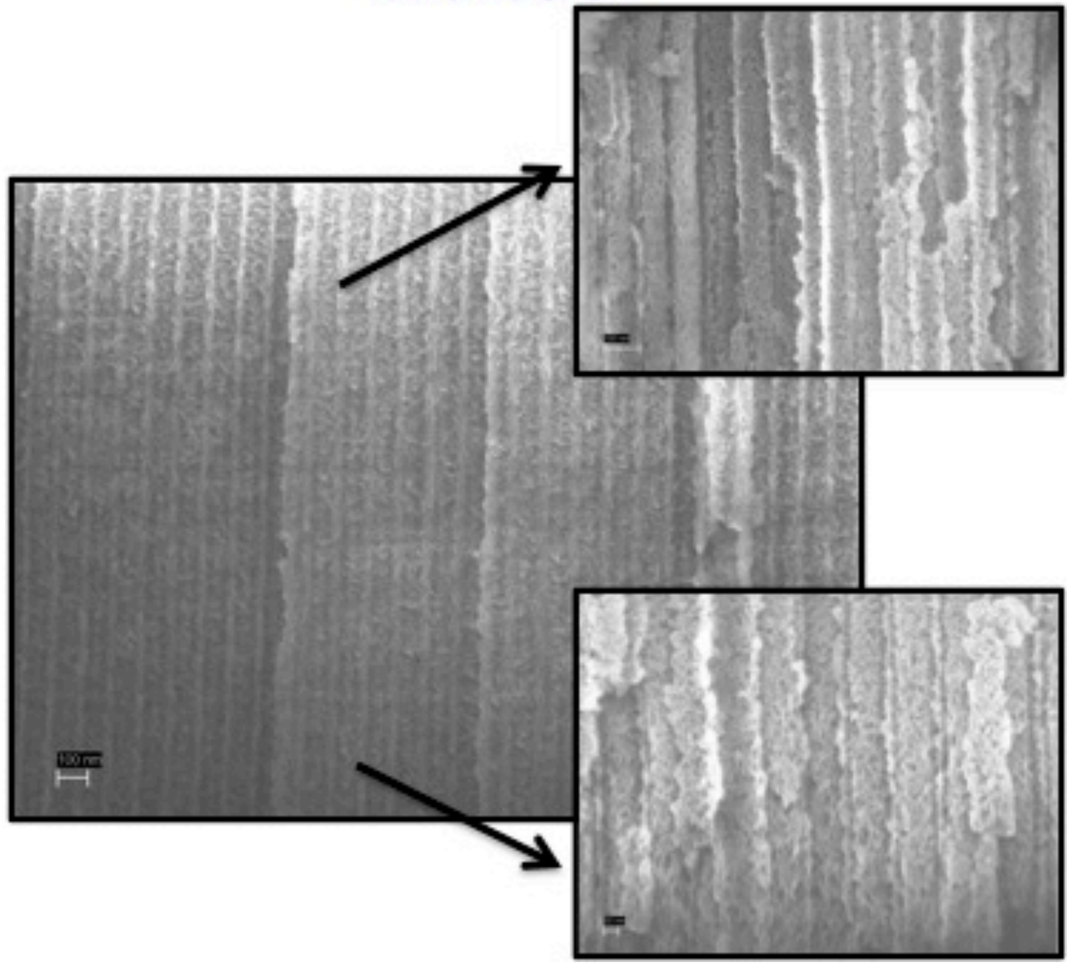
AAO template: Aspect ratio ~ 200



Empty vias before assembly

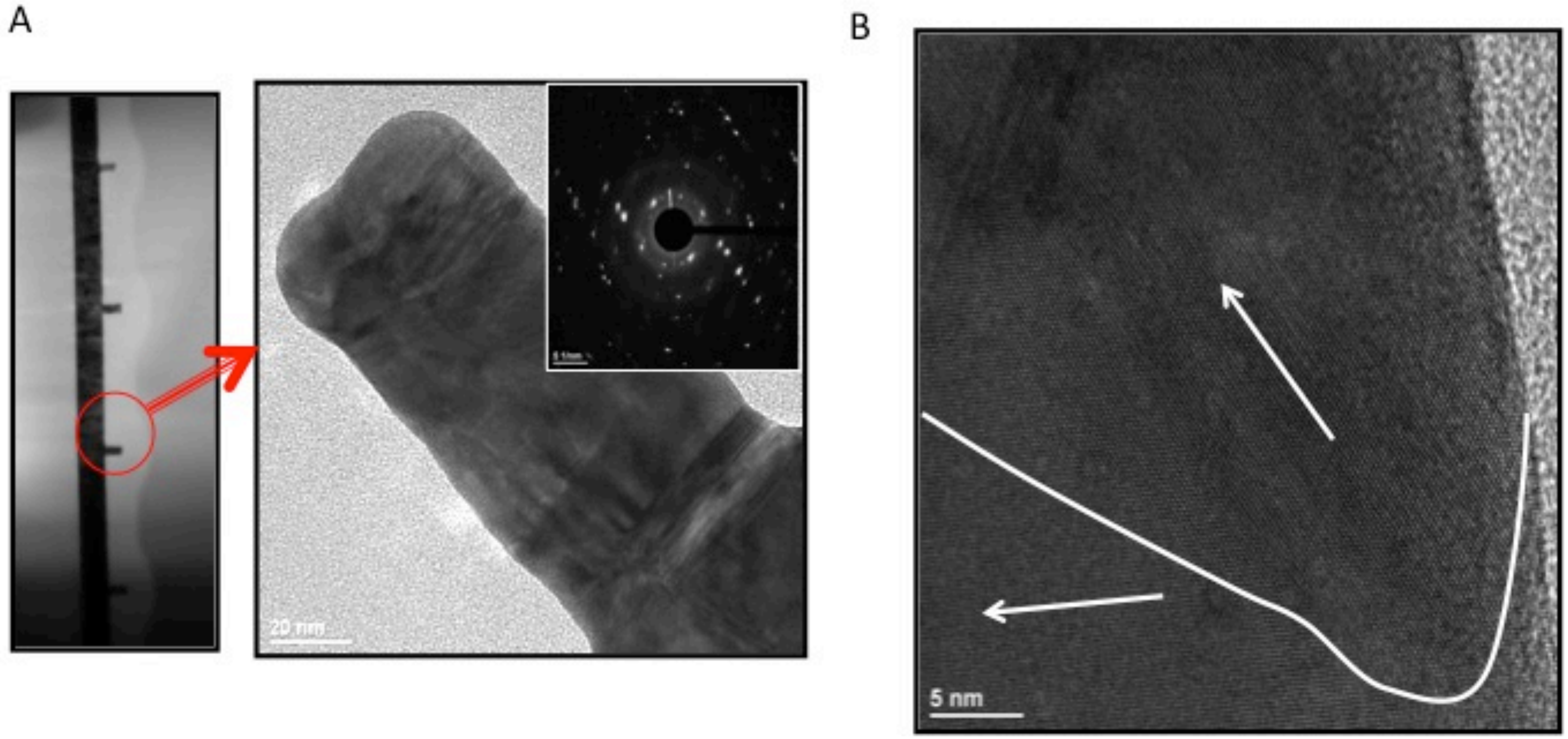


Vias after assembly and fusion



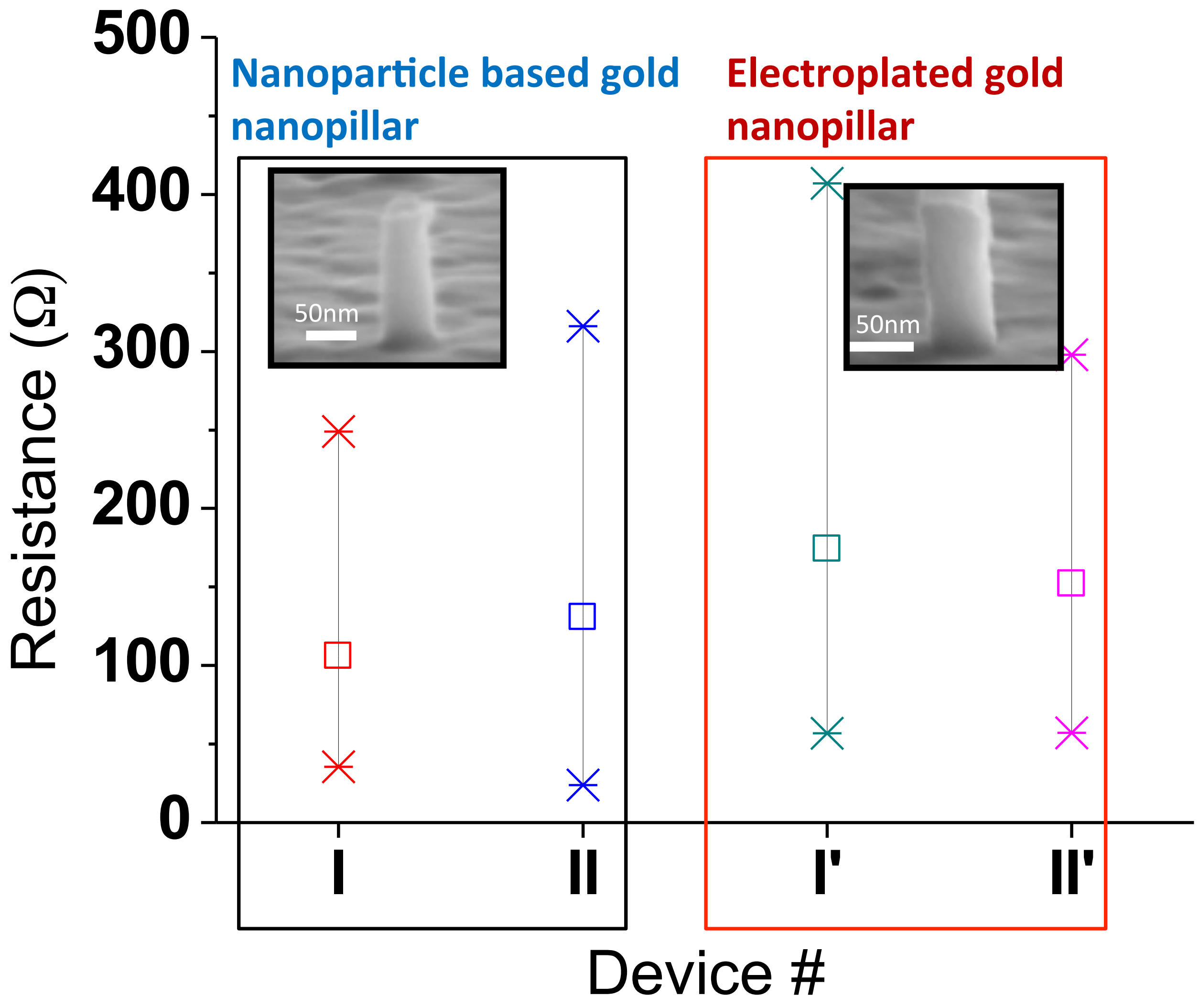
- ➢ **Interconnects can be fabricated in very high aspect ratio vias (e.g. 50nm diameter, 10 mm length).**
- ➢ **Promising for the fabrication of global/wafer packaging level interconnects.**

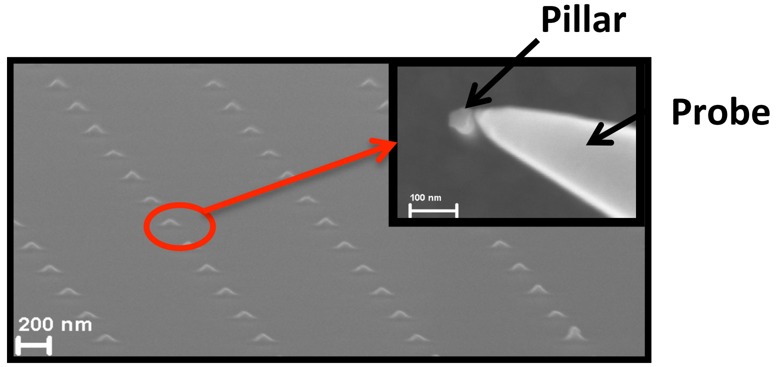
Material properties



- **TEM shows that NPs completely fuse without any voids or gaps.**
- **Nanopillars have polycrystalline nature.**

Electrical Properties

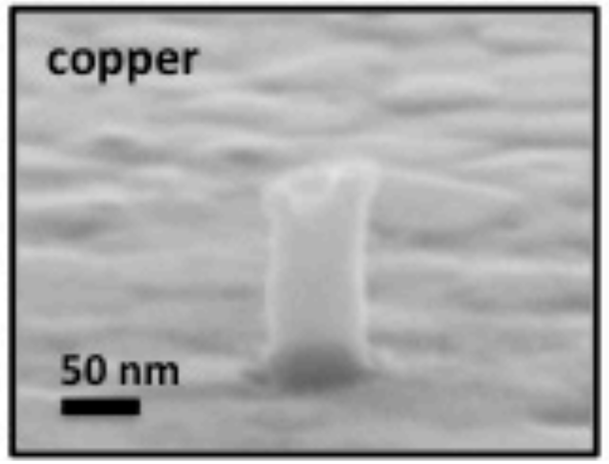


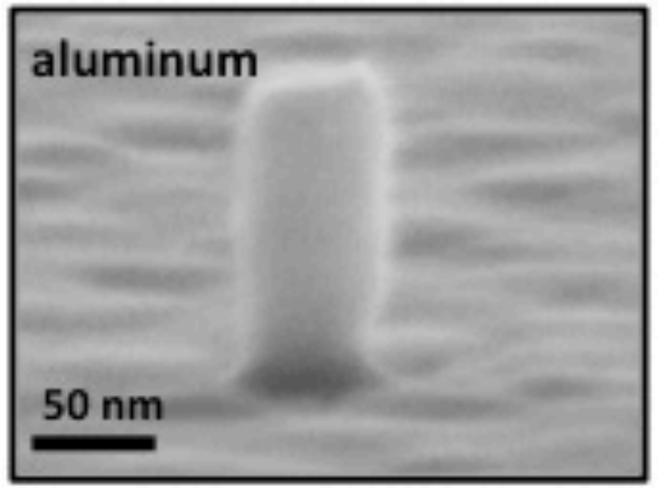


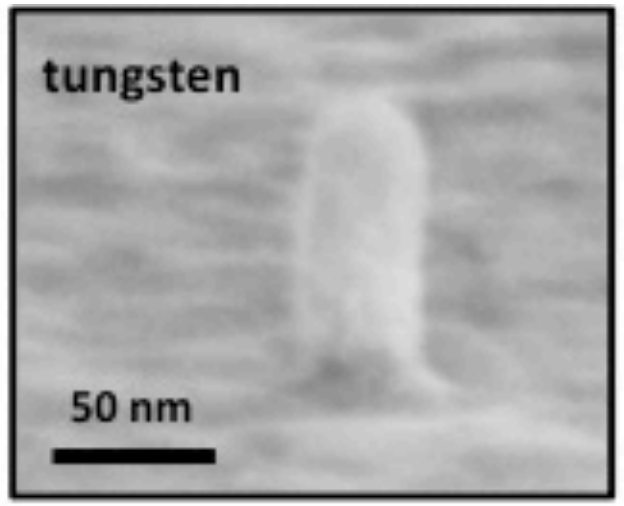
Measurements were performed
using a scanning electron
microscopy in-situ nanomanipulator

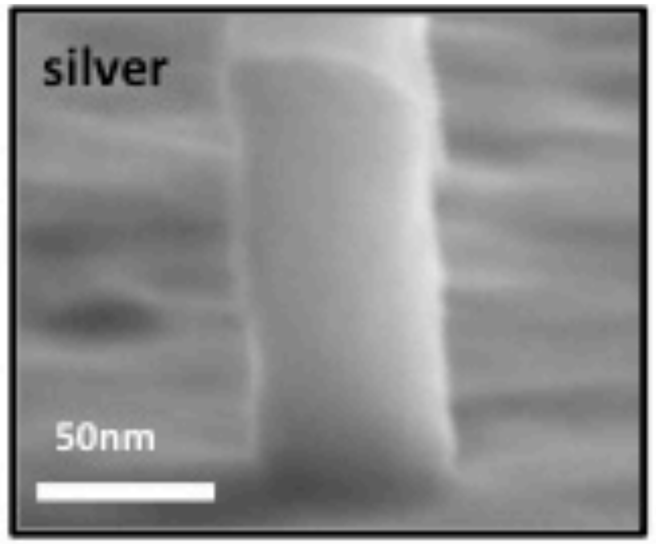
- ➢ **Similar or better resistivity values were observed (~ 10-7 Ω·m) from the nanopillars fabricated by nanoparticles and conventional electroplating.**
- ➢ **The obtained resistivity was only 1 order of magnitude higher ($1.96\times10^{-7}\Omega\cdot m$) from bulk gold resistivity.**
- ➢ **Tungsten resistivity is similar to CVD tungsten.**

Capability of fabricating various materials









Acknowledgement

This work has been performed at Northeastern University.

NSF

Northeastern
UNIVERSITY


flex
LIVE SMARTER

Global Scale & Reach

$26 billion
company

52 million
sq. ft. of manufacturing and services space

>1,000
global customers

200,000+
employees

30
Countries

1.2 million
active components

100+
locations

14,000
active global suppliers

2,500
design engineers

Global Design & Innovation Presence

9 Product Introduction Centers | 25+ Design Centers | 2500 Design Engineers

Insight across industries

Healthcare

$2 Billion

Automotive

$2 Billion

Industrial

$1 Billion

Home Appliances

$1 Billion

Capital Equipment

$1 Billion

Energy

$1 Billion

Datacom

$3 Billion

Telecom

$3 Billion

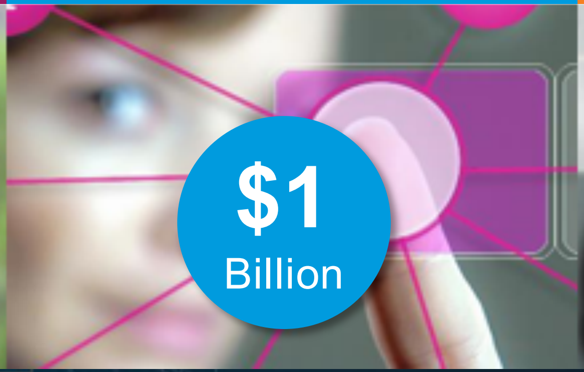
Server/Storage

$3 Billion

Wearables

$1 Billion

Connected Living



$1 Billion

Smartphones

$3 Billion

Flex Sustainable Innovation

Access to new & tested technology building blocks

Development partner ecosystem

Improved product reliability

Accelerate time to market

Early stage engagement

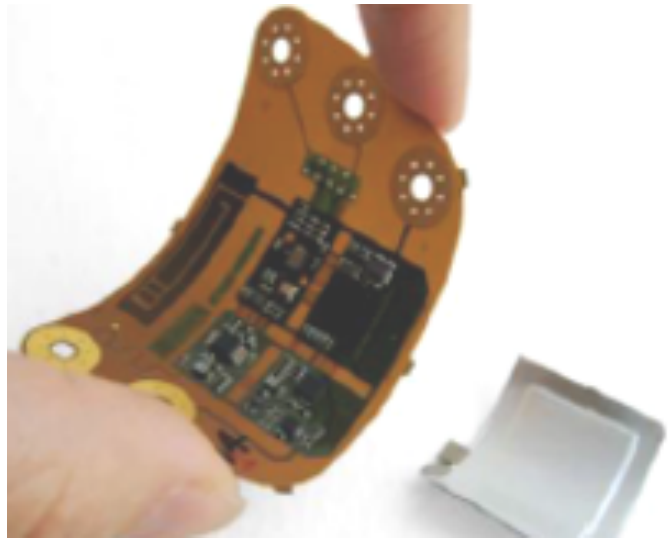
Entry into new & adjacent markets

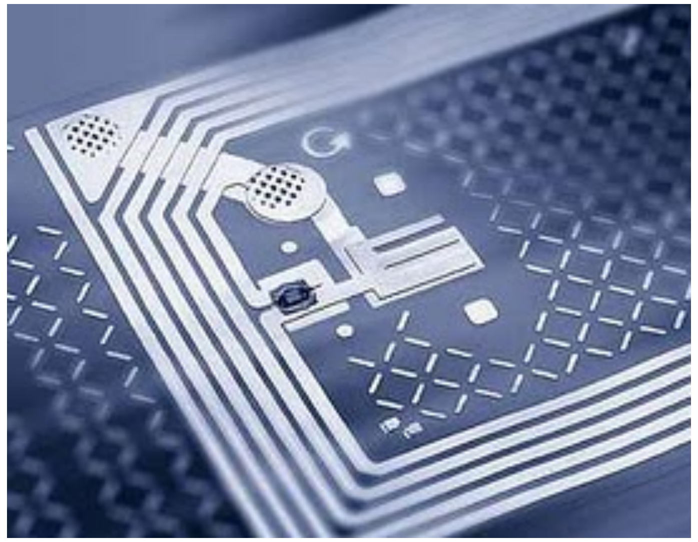
Experienced design & engineering teams

Flex Smart Products

Smart Technology Building Blocks


Biosensors

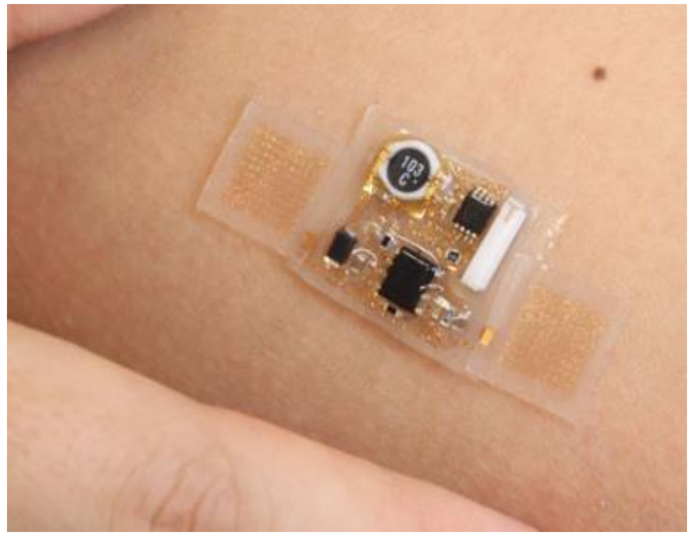

Flexible battery & PCB


Printed electronics


Durable/Disposable attachments

Wireless interface


Soft encapsulation


Biocompatible substrates

Displays & GUI

Flex Boston Innovation Center

Overview

A concepting, design & short run production facility to support the region
innovation economy from large multinational customers to startups.

Focus areas include

Health, Robotics, Textile & Apparel,
Energy, Mobility

Equipment includes

3D printers & modeling,
CNC machining (metal, plastic, foam)
High precision injection molding
Laser metal cutter
Textile Engineering

Space

17,000 sq ft to support product & system design, prototyping, assembly and testing

Flex Boston Innovation Center

CONCEPTING

Exploratory and collaborative development of early stage product concepts for new market applications

DESIGN AND ENGINEERING

Collaborative ecosystem approach to reduce time to market for customers, technology partners, and universities

PROTOTYPING

17,000 square feet of engineering/prototyping space to support product and system design, prototyping, assembly, and testing

MANUFACTURING

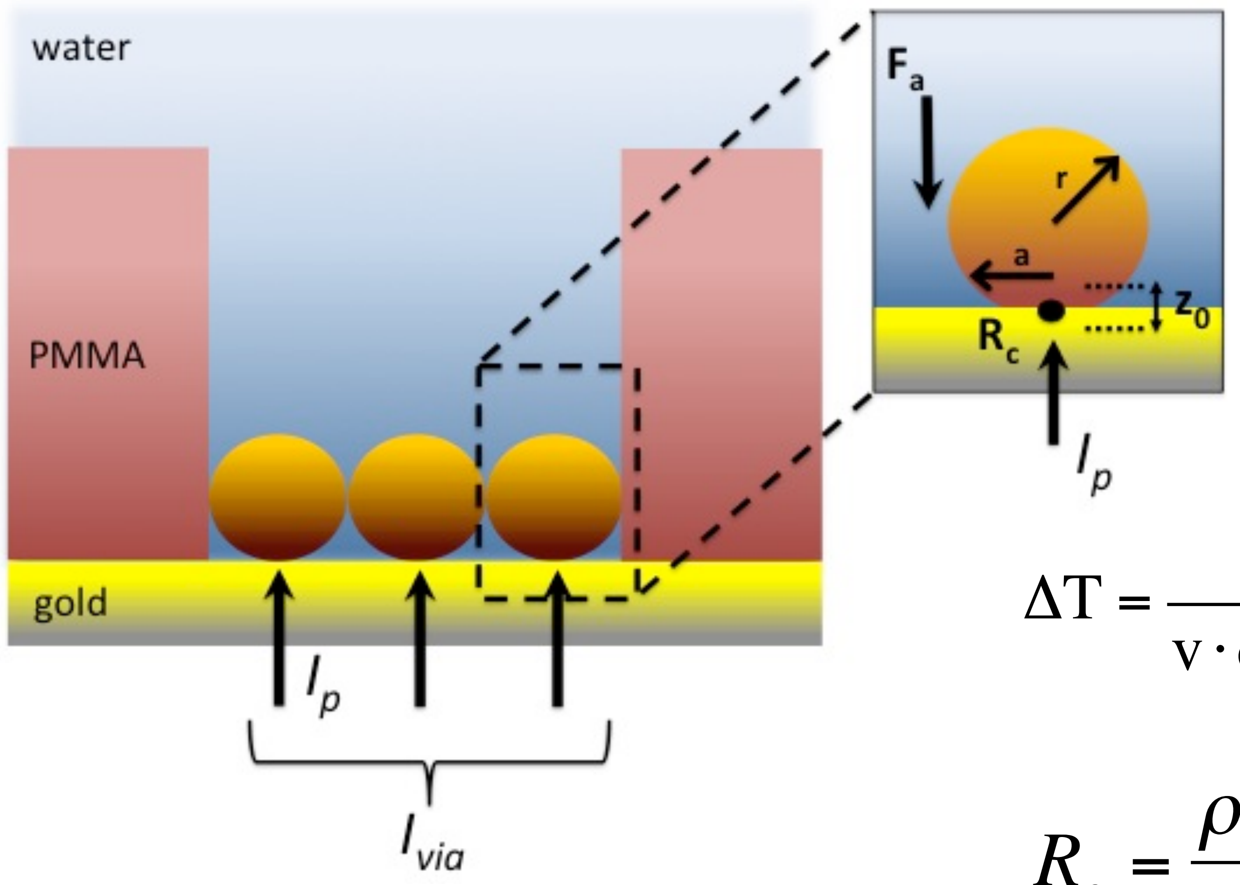
Assembly line and shipping station for your first product sample to your first hundred test units

Thank You

Comparison with other interconnect fabrication methods

Interconnect fabrication method	Material independent	Room temperature	Atmospheric pressure	Seed layer requirement	Chemical additives requirement
Electroplating	No	Yes/No	Yes	Yes	Yes
Thin film deposition	No	No	No	Yes/No	Yes/No
Directed nanoparticle assembly	Yes	Yes	Yes	No	No

Fusion Mechanism



$$\Delta T = \frac{Q}{v \cdot c_{v,gold}}$$

$$R_c = \frac{\rho_c \cdot z_0}{A_c}$$

F_a : van der Walls force
z_0 : the separation distance between the particle (0.4nm)
a : the contact radius
R_c : the contact resistance
I_p : the magnitude of the applied current

Particle size	5nm	20nm	50nm
Resistivity at contact (ohm·m)	1.50E-04	6.00E-06	1.40E-07
Contact diameter (nm)	7.20E-09	1.70E-08	2.70E-08
Contact length (nm)	4.00E-10	4.00E-10	4.00E-10
Current (A)	1.62E-03	3.50E-03	3.50E-03
Resistance (ohm)	1.47E+03	1.19E+01	9.79E-02
Joule heating (W)	9.67E-15	6.58E-16	5.27E-16
Temperature increase (C)	5.93E+02	6.31E+01	3.23E+00
Result	**fused**	**partially fused**	**not fused**

- **The localized Joule heating due to the applied current fuses the 5nm particles.**
- **Small size particles (<10nm) have much lower melting temperature compared to their bulk melting points.**
- **The amount of current was not enough to completely fuse 20 and 50nm particles.**